ABSTRACT OF THE DISCLOSURE

A semiconductor device capable of preventing defective embedding of an insulator and improving the withstand voltage (dielectric strength) of an element isolation region is obtained. This semiconductor device comprises a semiconductor substrate having a main surface and an element isolation trench formed on the main surface of the semiconductor device, while the trench width of an upper end of the element isolation trench is larger than the trench width of a bottom surface and the length of a side surface located between the upper end and an end of the bottom surface is larger than the length of a straight line connecting the upper end and the end of the bottom surface. Thus, the element isolation trench is so formed that the trench width of the upper end is larger than the trench width of the bottom surface, whereby an insulator can be readily embedded in the element isolation trench. Thus, the insulator can be prevented from defective embedding. Further, the element isolation trench is so formed that the length of the side surface located between the upper end and the end of the bottom surface is larger than the length of the straight line connecting the upper end and the end of the bottom surface, thereby improving the withstand voltage of the element isolation region as compared with a case of forming the side surface located

between the upper end and the end of the bottom surface in a tapered manner.